IN THE CLAIMS:

Please amend the claims as follows:

1-63. (Canceled)

64. (Currently Amended) A system, comprising,

~~a first computer coupled to a second computer;~~

a ~~second~~ computer configured to couple[[d]] to an emulator, wherein the emulator is configured to emulate a design of an integrated circuit having a network interface;

wherein the ~~first~~ computer is configured to receive ~~send~~ one or more data packets ~~to the second computer~~ at a first transmission rate ~~speed~~;

wherein the ~~second~~ computer is configured to:

~~receive the data packets;~~

buffer the data packets; and

send data contained in ~~corresponding to~~ the buffered data packets to the emulator at a second transmission rate ~~speed~~, wherein the second transmission rate ~~speed~~ is slower than the first transmission rate ~~speed; and wherein the emulator is configured to receive and process the sent data according to the design of the integrated circuit.~~

65. (Currently Amended) The system of claim 64, wherein the emulator is configured to receive and process the sent data according to the design of the integrated circuit.

~~further comprising a third computer coupled to the emulator via a bus;~~

~~wherein the emulator is configured to send the processed data to the third computer~~[[.]]

66. (Currently Amended) The system of claim 65[[4]], wherein the ~~second~~ computer is configured to, for each incoming data packet:

examine that data packet;

determine if that data packet is addressed to the emulator; and

if that data packet is addressed to the emulator, buffer that data packet and send data ~~corresponding to~~ contained in the buffered packet to the emulator.

67. (Currently Amended) The system of claim 64, wherein the emulator is incapable of receiving and processing data sent at the first transmission rate ~~speed~~.

68. (Currently Amended) The system of claim 65[[4]], wherein the emulator is implemented, at least in part, using field programmable gate arrays; and

wherein the field programmable gate arrays are operable to be programmed with a hardware model corresponding to the design of the integrated circuit.

69. (Currently Amended) The system of claim 64, wherein the ~~second~~ computer is further configured to repackage data from the buffered data packets;

wherein the repackaged data is the data the ~~second~~ computer is configured to send to the emulator at the second transmission rate ~~speed~~.

70. (Currently Amended) The system of claim 65[[4]], wherein the ~~second~~ computer is further configured to log data corresponding to received data and/or sent data in a log file.

71. (Canceled)

72. (Currently Amended) The system of claim 65, further comprising another ~~wherein the first~~ computer that is configured to generate the one or more packets received at ~~to be sent to~~ the ~~second~~ computer,[[; and]] wherein the generated packets are variable in size.

73. (Currently Amended) A method, comprising:

a first computer receiving a plurality of data packets at a first transmission rate ~~speed~~, wherein the data packets are received over a network connection;

the first computer buffering one or more of the plurality of data packets; and

the first computer sending data contained in ~~corresponding to~~ the buffered data packets to an emulator, wherein the emulator is configured to emulate a design of an integrated circuit ~~to be~~ used as a component of a network communication device, and wherein said sending occurs at a second transmission rate that is ~~speed~~ slower than the first transmission rate. ~~speed~~;

~~the emulator receiving and processing the data sent by the first computer, wherein said processing is performed, at least in part, according to the design of the integrated circuit; and~~

~~the emulator sending data corresponding to the received and processed data to a second computer~~[[.]]

74. (Previously Presented) The method of claim 73, wherein the data sent to the second computer is usable to debug the design of the integrated circuit; and

wherein the network connection is an ethernet connection.

75. (Previously Presented) The method of claim 73, further comprising:

the first computer repackaging data from the buffered data packets;

wherein the repackaged data is the data sent from the first computer to the emulator.

76. (Currently Amended) The method of claim 73, further comprising:

the emulator receiving and processing the data sent by the first computer, wherein said processing is performed, at least in part, according to the design of the integrated circuit.

~~the first computer logging contents of one or more of the received data packets in a log file~~[[.]]

77. (Currently Amended) The method of claim 76[[3]], further comprising the emulator sending data corresponding to the received and processed data to a second computer.

~~first computer logging the sent data in a log file~~[[.]]

78. (Currently Amended) The method of claim 77[[3]], wherein the emulator is configured to emulate a network interface card of the second computer; and

wherein the data is sent to the second computer via a bus coupled to the emulator.

79. (Currently Amended) The method of claim 73, further comprising the first computer, for each data packet received:

examining that data packet;

determining if that data packet is addressed to the emulator, wherein the emulator is configured to emulate a network interface card ~~of the second computer~~; and

if that data packet is addressed to the emulator, buffering that data packet and sending data contained in ~~corresponding to~~ the buffered packet to the emulator at the second transmission rate ~~speed~~.

80. (Currently Amended) The method of claim 76[[3]], wherein the emulator is implemented, at least in part, using field programmable gate arrays; and

wherein the field programmable gate arrays are operable to be programmed with a hardware model corresponding to the design of the integrated circuit.

81. (New) A tangible computer-readable medium having instructions stored thereon that are executable to cause a computer system to perform operations that include:

receiving, at a first transmission rate, one or more data packets sent from a different computer system;

buffering the received data packets within a memory of the computer system;

at a second transmission rate that is slower than the first transmission rate, sending data contained in the buffered data packets to an emulator that is configured to receive and process the sent data according to a design of an integrated circuit having a network interface.

82. (New) The tangible computer-readable medium of claim 81, wherein the operations further include, for each data packet received by the computer system:

examining that data packet;

determining if that data packet is addressed to the emulator; and

buffering that data packet and sending data contained in that buffered packet to the emulator only if that data packet is addressed to the emulator.

83. (New) The tangible computer-readable medium of claim 81, wherein the emulator is implemented, at least in part, using field programmable gate arrays to emulate the design of the integrated circuit.

84. (New) The tangible computer-readable medium of claim 81, wherein the operations further include repackaging the data contained in the buffered data packets prior to sending the data to the emulator at the second transmission rate.

85. (New) The tangible computer-readable medium of claim 81, wherein the emulator is configured to receive and process data sent at the second transmission rate, but is not configured to receive and process data sent at the first transmission rate.